

What is claimed:

- 1 1. A method for manufacturing a semiconductor device having a trench
2 isolation region, the method comprising the steps of:
3 (a) forming a trench in a semiconductor layer;
4 (b) forming a dielectric layer that fills the trench; and
5 (c) conducting a thermal treatment of the dielectric layer, wherein the thermal
6 treatment is conducted at temperatures of at least 1050°C.
- 1 2. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 1, wherein, in the step (b), the dielectric layer is formed
3 with a film density of at least 2.1g/cm³.
- 1 3. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 1, wherein the temperature of the thermal treatment is
3 1100°C or higher.
- 1 4. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 1, wherein the temperature of the thermal treatment is in
3 the range of 1050°C to 1250°C.
- 1 5. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 1, wherein the dielectric layer is formed by a high
3 density plasma CVD method.
- 1 6. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 1, further comprising the step (d) of forming a well in the
3 semiconductor layer, and the step (c) is conducted before the step (d).

1 7. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 1, wherein the trench includes sidewall surfaces and a
3 bottom surface, the method further comprising of thermally oxidizing the sidewall surfaces
4 and the bottom surface of the trench.

1 8. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 7, wherein the thermally oxidizing the sidewall surfaces
3 and the bottom surface of the trench is carried out at a temperature in the range of at 700°C
4 to 1150°C.

1 9. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 7, wherein the thermally oxidizing the sidewall surfaces
3 and the bottom surface of the trench is carried out at a temperature in the range of at 950 to
4 1150°C.

1 10. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 7, wherein the thermally oxidizing the sidewall surfaces
3 and the bottom surface yields an oxidation layer having a thickness in the range of 10 nm to
4 100 nm.

1 11. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 1, wherein the semiconductor layer comprises an
3 epitaxial growth layer formed on a semiconductor substrate.

1 12. A method for manufacturing a semiconductor device having a trench
2 isolation region according to claim 11, wherein the epitaxial growth layer has a thickness of
3 at least 2 μm .

1 13. A method for manufacturing a semiconductor device having a trench isolation
2 region according to claim 1, wherein the trench is formed with a trench width of no greater
3 than 0.35 μm .

1 14. A method for manufacturing a semiconductor device having a trench
2 isolation region, the method comprising:
3 forming a trench in a semiconductor layer;
4 forming a dielectric layer in the trench; and
5 heating the dielectric layer at a temperature of at least 1050°C.

1 15. A method as in claim 14, wherein the trench includes sidewalls and a bottom
2 surface, the method further comprising:
3 forming a trench oxide layer on the sidewalls and bottom of the trench prior to
4 forming the dielectric layer in the trench.

1 16. A method as in claim 15, wherein the trench oxide layer is formed by
2 oxidizing the sidewalls and bottom surface, and the trench oxide layer is formed to have a
3 thickness in the range of 10 nm to 100 nm.

1 17. A method as in claim 14, wherein the heating the dielectric layer is carried
2 out for a time in the range of 20 minutes to 120 minutes at a temperature in the range of
3 1050°C to 1200°C.

1 18. A method as in claim 14, further comprising forming at least one transistor
2 adjacent to the trench isolation region, the at least one transistor being formed after heating
3 the dielectric layer at a temperature of at least 1050°C.

1 19. A method for manufacturing a semiconductor device including a trench
2 isolation region, the method comprising:
3 forming a first layer on a semiconductor substrate;
4 forming a polishing stopper layer above the first layer;
5 forming at least one trench by etching the first layer while using the polishing
6 stopper layer as a mask;
7 forming a dielectric layer in and above the trench; and
8 planarizing the dielectric layer using the polishing stopper layer as a stopper.

1 20. A method as in claim 19, wherein the first layer comprises an epitaxial
2 growth layer.

1 21. A method as in claim 19, further comprising removing the polishing stopper
2 layer after planarizing the dielectric layer.

1 22. A method as in claim 19, further comprising oxidizing at least a portion of
2 the first layer in the at least one trench prior to forming the dielectric layer in and above the
3 trench.

1 23. A method as in claim 22, further comprising forming a pad layer between the
2 first layer and the polishing stopper layer.

1 24. A method as in claim 21, further comprising subjecting the dielectric layer to
2 a thermal treatment at a temperature of at least 1050°C after removing the polishing stopper
3 layer.

1 25. A method as in claim 24, wherein the thermal treatment is carried out in an
2 atmosphere comprising 0.1 volume % to 10 volume % oxygen.

1 26. A method as in claim , wherein the dielectric layer is formed using high
2 density plasma chemical vapor deposition.

1 27. A semiconductor device including a trench isolation region and transistor
2 element regions, comprising:
3 a semiconductor substrate;
4 a first layer formed on the semiconductor substrate;
5 a trench isolation region formed in the first layer; the trench isolation region
6 including a oxide layer and a dielectric material layer therein; and
7 transistor element regions separated by the trench isolation region.

1 28. A device as in claim 27, wherein the first layer comprises an epitaxial growth
2 layer.

1 29. A device as in claim 27, wherein the dielectric material layer comprises a
2 material having a density of at least 2.1g/cm^3 .

1 30. A device as in claim 27, wherein the dielectric material layer comprises a
2 material having a density of at least 2.3g/cm^3 .

1 31. A semiconductor device including a trench isolation region, comprising:
2 a semiconductor substrate;
3 an epitaxial growth layer on the semiconductor substrate;
4 a trench provided in the epitaxial growth layer;
5 an annealed dielectric layer in the trench;
6 a trench oxide film formed between the epitaxial growth layer and the dielectric
7 layer; and
8 transistor element regions separated by the trench isolation region.